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EXAMINER	
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ART UNIT	PAPER NUMBER
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,395	EGERER, JENS	
	Examiner	Art Unit	
	Michael Rutland-Wallis	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21 and 23-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21 and 23-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/18/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant translations of the abstracts of the previously submitted German patent documents have been received and therefore the documents have been considered.

Applicant's amendments to the specification have been entered and the previous objection is hereby withdrawn.

Applicant's amendments to claim 17 are fully responsive to the to withdraw both the 112 rejection and claim objection.

Applicant's arguments, filed 5/18/2007, with respect to the Barber rejection have been fully considered and are persuasive. The Barber rejection has been withdrawn.

Applicant's arguments with respect to the Nishikawa rejection filed 5/18/2007 have been fully considered but they are not persuasive. Applicant Alleges the failure of Nishikawa to teach the limitations added to claim 1 previously found in claim 22. Citing particularly there is no teaching or suggestion in Nishikawa that a second operating mode is possible nor is there any teaching or suggestion as to how the components would be connected to a different path than the assigned path.

In response Nishikawa teaches components may be assigned to more than one path (paragraph 0020). This configuration is shown is at least figure 2A. Nishikawa describes (paragraph 0096) voltage VDD1 or voltage VDD2 is supplied to the components 207e through 209e; i.e. the components belong or may be supplied power

from a first supply in a first mode when VDD1 is supplying the power or the power may be supplied from a second source in a second mode when VDD2 is supplying the power. Therefore there is a teaching in Nishikawa of that a change between power supplies takes place during different modes of operation.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11, 18-19, 23-25 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishikawa et al. (U.S. Pub. No. 2004/0094820)

With respect to claim 1 Nishikawa teaches a system (Fig. 2A or 2B) comprising first semiconductor device (for example 208e), and second semiconductor device (209e), wherein the first semiconductor device (for example 208e) comprises a voltage supply means (VDD1), characterized in that said voltage supply means of said first semiconductor device is connected (signal path 21p in Fig. 2A) to said second semiconductor device, so that said voltage supply means of said first semiconductor device can provide (see paragraph 0096) a supply voltage for said second semiconductor device wherein, in a first operating mode (voltage supplied from VDD2) of said second semiconductor device, said voltage supply means (VDD2) of said

second semiconductor device (209e) provides the supply voltage for said second semiconductor device (209e), and wherein, in a second operating mode (voltage supplied from VDD1) of said second semiconductor device, said voltage supply means (VDD1) of said first semiconductor device (208e) provides the supply voltage for said second semiconductor device.

With respect to claim 2 Nishikawa teaches said first semiconductor device and said second semiconductor device are arranged in the same block (circuit block item 2Ca). Nishikawa does not teach the circuitry is contained within a housing, semiconductor components are typically found a housing and not exposed. It would have been obvious to one of ordinary skill in the art at the time of the invention to put the circuit block of Nishikawa into a housing if in fact such a housing is not utilized by Nishikawa in order to protect the semiconductor.

With respect to claim 3 Nishikawa teaches the first and second semiconductor devices are arranged in a stacked manner (see arrangement of components in Fig. 1 or 2 from top to bottom and left to right)

With respect to claims 4-7 Nishikawa is silent on the on the detailed nature of the components and whether said components are plug mountable, DIL, SMD or PGA. As Applicant admits in page 2 lines 24-31 of the disclosure semiconductors are usually incorporated in appropriate housings e.g. SMD, plug mountable, DIL, PGA etc... It would have been obvious to one of ordinary skill in the art at the time of the invention to connected semiconductors as appropriate to the housing in order to provide a simple and reliable connection to other connected semiconductors.

With respect to claim 8 Nishikawa teaches the system and components comprise one semiconductor (item 2Ca).

With respect to claim 9 Nishikawa teaches said one further semiconductor device is arranged in the same circuit block (2Ca), as the first and said second semiconductor devices (208e and 209e). Nishikawa does not teach the circuitry is contained within a housing, semiconductor components are typically found a housing and not exposed. It would have been obvious to one of ordinary skill in the art at the time of the invention to put the circuit block of Nishikawa into a housing if in fact such a housing is not utilized by Nishikawa in order to protect the semiconductor.

With respect to claim 10 Nishikawa teaches the voltage supply means (VDD) of said first semiconductor device (208e) is additionally also connected (via path 21p) to said one or to said several further semiconductor device, so that said voltage supply means (VDD1) of said first semiconductor device can additionally provide a supply voltage for said one or said several further semiconductor device (see paragraph 0096).

With respect to claim 11 Nishikawa teaches first semiconductor device (208e) comprises a further voltage supply means (VDD2) that is connected to said one or said several further semiconductor device, so that said further voltage supply means of said first semiconductor device (208e) can provide a supply voltage for said one or said several furthers semiconductor device (see paragraph 0096 or Fig. 2A).

With respect to claim 18 Nishikawa teaches the voltage supply means (VDD) provide a voltage supply for said first semiconductor device (208e).

With respect to claim 19 Nishikawa teaches the voltage supply means generates the respective supply voltage from an external voltage (supplied to the VDD terminal or pad).

With respect to claim 23 Nishikawa teaches the second semiconductor device (209e) comprises a voltage supply means (VDD2), and wherein, in a first operating mode (voltage supplied from VDD2) of said second semiconductor device, said voltage supply means (VDD2) of said second semiconductor device (209e) provides the supply voltage for said second semiconductor device (209e), and wherein, in a second operating mode (voltage supplied from VDD1) of said second semiconductor device, said voltage supply means (VDD1) of said first semiconductor device (208e) provides the supply voltage for said second semiconductor device.

With respect to claims 24 and 25 Nishikawa does not teach the second operating mode is a standby mode or refresh mode. It would have been obvious to one of ordinary skill in the art at the time of the invention to name the modes refresh or standby mode in order to distinguish between the different modes.

With respect to claim 27 Nishikawa teaches a device function adjusting means (see paragraph 0094-0095 where Nishikawa describes the stepping down of voltage), in particular an appropriate fuse (bonding wire connecting components item 208e and 209e), is provided on said first semiconductor device (208e), by means of which it is determined whether the corresponding semiconductor device is to assume the function of said first semiconductor device.

With respect to claim 28 Nishikawa teaches the voltage supply means (VDD) of said first semiconductor device (208e) is connected to a corresponding pad (see in Fig. 2) of said first semiconductor device (208e).

With respect to claim 29 Nishikawa teaches the pad of said first semiconductor device is connected to a corresponding pad of said second semiconductor device, which said voltage supply means of said second semiconductor device can be connected to (see Fig. 2).

With respect to claim 30 Nishikawa teaches the pad of said first semiconductor device is connected directly to the corresponding pad of said second semiconductor device by means of an appropriate bonding wire (see Fig. 2).

With respect to claim 31 Nishikawa teaches the pad of said first semiconductor device is connected indirectly to the corresponding pad of said second semiconductor device. Nishikawa does not teach the use of an interposer, however the interconnection seen in Fig. 1 between circuit blocks. It would have been obvious to one of ordinary skill in the art at the time of the invention to use an interposer or other connection means to connect the circuit blocks in order to provide a reliable connection between circuit blocks.

Claims 12-17, 20-21, 26 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishikawa et al. (U.S. Pub. No. 2004/0094820) in view of Odisho et al. (U.S. Pat. No. 5,758,100)

With respect to claim 12-14 Nishikawa is silent on the on the detailed nature of the components specifically whether the first semiconductor device is a memory device.

Odisho teaches a typical semiconductor integrated circuit (item 202) comprising a memory device (RAM module item 212). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the semiconductor voltage supply configuration of Nishikawa with memory devices as seen in Odisho in order to supply memory modules with variable voltage requirements.

With respect to claim 15 Nishikawa as modified by Odisho are silent on whether the RAM is DRAM (dynamic RAM) as understood by the examiner the RAM modules are DRAM modules, while not explicitly stated by Odisho, however should one content otherwise, It would have been obvious to one of ordinary skill in the art at the time of the invention to use DRAM modules in order to supply typical memory modules is a computer with voltage.

With respect to claim 16 Odisho teaches the memory devices items 212 and additional circuitry may comprise a graphics card or a network card (col. 2 line 55) know to one of ordinary skill in the art to utilize ROM.

With respect to claim 17 Nishikawa as modified by Odisho teach said memory devices, are addressable memory circuits and are made up of transistors, and therefore constitute an array of programmable logic devices.

With respect to claims 20 and 21 Nishikawa teaches the voltage supply means (VDD) comprise a voltage regulating means and charge pump to control the voltage to memory modules with different voltage requirements.

With respect to claim 26 Nishikawa does not teach the first operating mode is a working mode, in which external access to the second semiconductor device is

performed. Odisho teaches the components are pluggable memory modules. It would have been obvious to one of ordinary skill in the art at the time of the invention to provide external access to the semiconductor device in order to remove the module when the memory module is no longer needed.

With respect to claim 31 and 32 Nishikawa as modified by Odisho teaches the memory devices are functional memory devices and are fundamental memory devices.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-

272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MRW

7/6/07

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